- **Wide Gain-Bandwidth Product . . . 4 MHz**
- **High Slew Rate . . . 13 V/μs**
- **Fast Settling Time . . . 1.1 μs to 0.1%**
- **Wide-Range Single-Supply Operation . . . 4 V to 36 V**
- **Wide Input Common-Mode Range Includes Ground (V_{CC-})**
- **Low Total Harmonic Distortion . . . 0.02%**
- **Large-Capacitance Drive Capability . . . 10,000 pF**
- **Output Short-Circuit Protection**

D OR P PACKAGE
(TOP VIEW)

1OUT	1	8	V_{CC+}
1IN−	2	7	2OUT
1IN+	3	6	2IN−
V_{CC-}/GND	4	5	2IN+
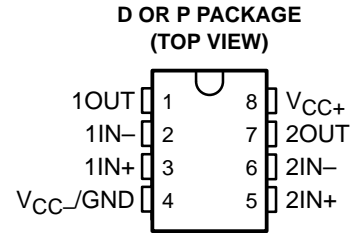
description/ordering information

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3472 operational amplifier. This device offers 4 MHz of gain-bandwidth product, 13-V/μs slew rate, and fast settling time, without the use of JFET device technology. Although the TL3472 can be operated from split supplies, it is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential (V_{CC-}). With a Darlington transistor input stage, this device exhibits high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

ORDERING INFORMATION

| T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (P)	Tube of 25	TL3472CP	TL3472CP
	SOIC (D)	Tube of 50	TL3472CD	3472C
		Reel of 2500	TL3472CDR	
−40°C to 105°C	PDIP (P)	Tube of 25	TL3472IP	TL3472IP
	SOIC (D)	Tube of 50	TL3472ID	Z3472
		Reel of 2500	TL3472IDR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

schematic (each amplifier)
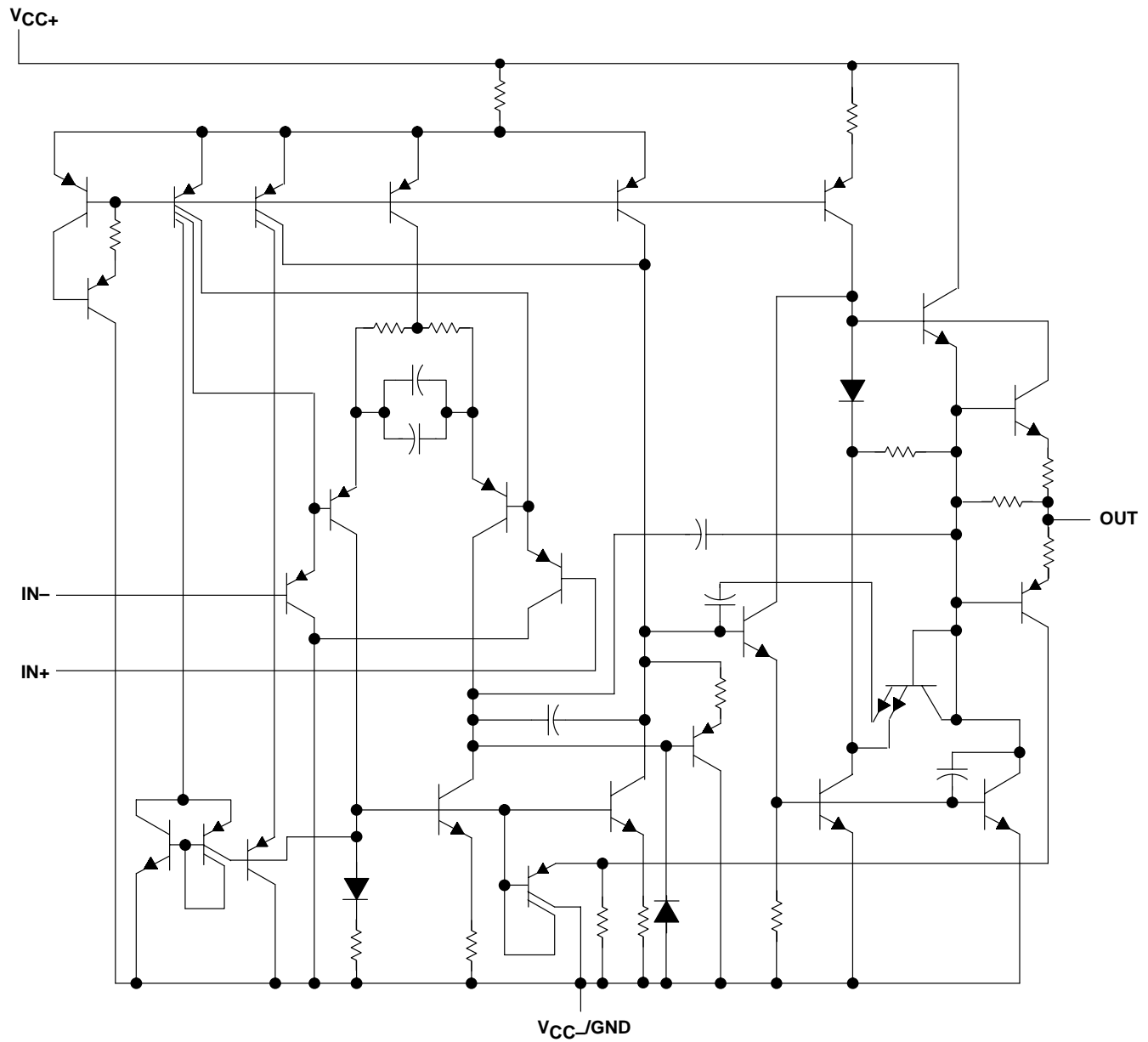
V_{CC+}

IN–

IN+

OUT

V_{CC}–/GND

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (see Note 1): V_{CC+} .... 18 V
V_{CC-} .... −18 V
Differential input voltage, V_{ID} (see Note 2) .... ±36 V
Input voltage, V_I (any input) .... $V_{CC\pm}$
Input current, I_I (each input) .... ±1 mA
Output current, I_O .... ±80 mA
Total current into V_{CC+} .... 80 mA
Total current out of V_{CC-} .... 80 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) .... Unlimited
Package thermal impedance, θ_{JA} (see Notes 4 and 5): D package .... 97°C/W
P package .... 85°C/W
Operating virtual junction temperature, T_J .... 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds .... 260°C
Storage temperature range, T_{stg} .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive input current can flow when the input is less than V_{CC-} − 0.3 V.
3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
4. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
5. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

			MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage		4	36	V
V_{IC}	Common-mode input voltage	V_{CC} = 5 V	0	2.8	V
		$V_{CC\pm}$ = ±15 V	−15	12.8	
T_A	Operating free-air temperature	TL3472C	0	70	°C
		TL3472I	−40	105	

electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP†	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0$, $V_O = 0$, $R_S = 50\ \Omega$	$V_{CC} = 5$ V	25°C		1.5	10	mV
			$V_{CC} = \pm15$ V	25°C		1.0	10	
				Full range‡			12	
$\alpha_{V_{IO}}$	Temperature coefficient of input offset voltage		$V_{CC} = \pm15$ V	Full range‡		10		µV/°C
I_{IO}	Input offset current		$V_{CC} = \pm15$ V	25°C		6	75	nA
				Full range‡			300	
I_{IB}	Input bias current		$V_{CC} = \pm15$ V	25°C		100	500	nA
				Full range‡			700	
V_{ICR}	Common-mode input voltage range	$R_S = 50\ \Omega$		25°C		−15 to 12.8		V
				Full range‡		−15 to 12.8		
V_{OH}	High-level output voltage	$V_{CC+} = 5$ V, $V_{CC-} = 0$, $R_L = 2\ k\Omega$		25°C	3.7	4		V
		$R_L = 10\ k\Omega$		25°C	13.6	14		
		$R_L = 2\ k\Omega$		Full range‡	13.4			
V_{OL}	Low-level output voltage	$V_{CC+} = 5$ V, $V_{CC-} = 0$, $R_L = 2\ k\Omega$		25°C		0.1	0.3	V
		$R_L = 10\ k\Omega$		25°C		−14.7	−14.3	
		$R_L = 2\ k\Omega$		Full range‡			−13.5	
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V, $R_L = 2\ k\Omega$		25°C	25	100		V/mV
				Full range‡	20			
I_{OS}	Short-circuit output current	Source: $V_{ID} = 1$ V, $V_O = 0$		25°C	−10	−34		mA
		Sink: $V_{ID} = −1$ V, $V_O = 0$			20	27		
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR}$(min), $R_S = 50\ \Omega$		25°C	65	97		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm} = \pm13.5$ V to ±16.5 V, $R_S = 100\ \Omega$		25°C	70	97		dB
I_{CC}	Supply current (per channel)	$V_O = 0$, No load		25°C		3.5	4.5	mA
				Full range‡		4.5	5.5	
		$V_{CC+} = 5$ V, $V_O = 2.5$ V, $V_{CC-} = 0$, No load		25°C		3.5	4.5	

† All typical values are at $T_A = 25°C$.
‡ Full range is 0°C to 70°C for the TL3472C device and −40°C to 105°C for the TL3472I device.

operating characteristics, $V_{CC\pm} = \pm15$ V, $T_A = 25°C$

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR+	Positive slew rate	$V_I = -10$ V to 10 V, $R_L = 2$ kΩ, $C_L = 300$ pF	$A_V = 1$	8	10		V/μs
SR−	Negative slew rate		$A_V = -1$		13		V/μs
t_S	Settling time	$A_{VD} = -1$, 10-V step	To 0.1%		1.1		μs
			To 0.01%		2.2		
V_n	Equivalent input noise voltage	f = 1 kHz, $R_S = 100$ Ω			49		nV/√$\overline{Hz}$
I_n	Equivalent input noise current	f = 1 kHz			0.22		pA/√$\overline{Hz}$
THD	Total harmonic distortion	$V_{O(PP)} = 2$ V to 20 V, $R_L = 2$ kΩ, $A_{VD} = 10$, f = 10 kHz			0.02		%
GBW	Gain-bandwidth product	f =100 kHz		3	4		MHz
BW	Power bandwidth	$V_{O(PP)} = 20$ V, $R_L = 2$ kΩ, $A_{VD} = 1$, THD = 5.0%			160		kHz
ϕ_m	Phase margin	$R_L = 2$ kΩ	$C_L = 0$		70		deg
			$C_L = 300$ pF		50		
	Gain margin	$R_L = 2$ kΩ	$C_L = 0$		12		dB
			$C_L = 300$ pF		4		
r_i	Differential input resistance	$V_{IC} = 0$			150		MΩ
C_i	Input capacitance	$V_{IC} = 0$			2.5		pF
	Channel separation	f = 10 kHz			101		dB
z_o	Open-loop output impedance	f = 1 MHz, $A_V = 1$			20		Ω

P (R-PDIP-T8)   **PLASTIC DUAL-IN-LINE**

0.400 (10,60)
0.355 (9,02)

8   5

0.260 (6,60)
0.240 (6,10)

1   4

0.070 (1,78) MAX

0.020 (0,51) MIN

0.200 (5,08) MAX

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ | 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)
Gage Plane

Seating Plane

0.010 (0,25) NOM

0.430 (10,92)
MAX

4040082/D 05/98

NOTES: A. All linear dimensions are in inches (millimeters).
            B. This drawing is subject to change without notice.
            C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN

0.050 (1,27)

0.020 (0,51) / 0.014 (0,35)

⊕ | 0.010 (0,25)Ⓜ

8

5

0.244 (6,20) / 0.228 (5,80)

0.157 (4,00) / 0.150 (3,81)

1

4

A

0.008 (0,20) NOM

Gage Plane

0.010 (0,25)

0°– 8°

0.044 (1,12) / 0.016 (0,40)

0.069 (1,75) MAX

0.010 (0,25) / 0.004 (0,10)

Seating Plane

◠ | 0.004 (0,10)

DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)
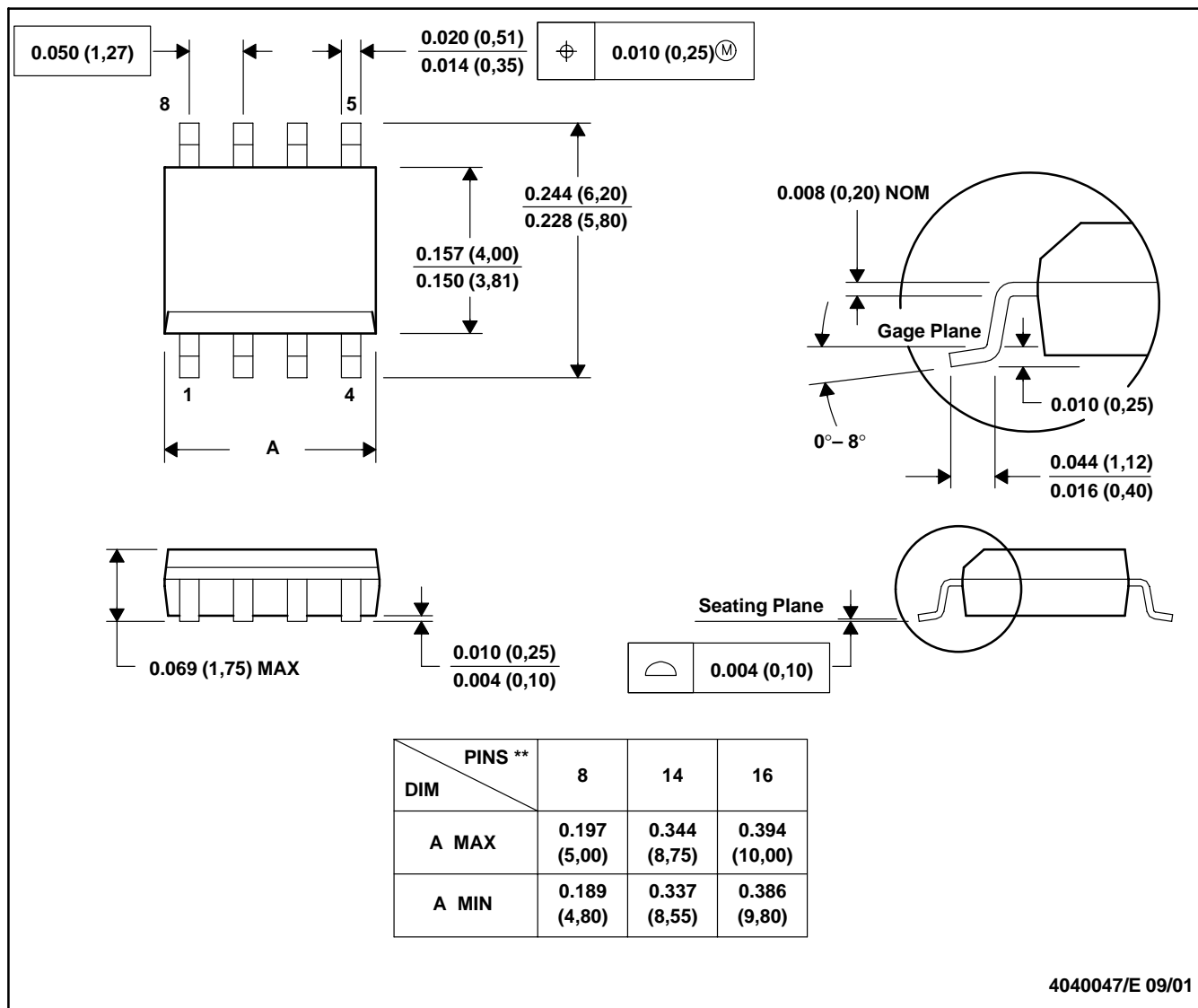
4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

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